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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): LU, Cam L.
et al.

Serial No.: 10/728,036

Filed: December 3, 2003

For: METHOD OF GENERATING AN EFFICIENT STUCK-AT FAULT AND TRANSITION DELAY FAULT TRUNCATED SCAN TEST PATTERN FOR AN INTEGRATED CIRCUIT DESIGN

Art Unit: 2825

Examiner: Siek, Vuthe

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

October 26, 2005 Julie Freiburger

DECLARATION UNDER 37 C.F.R. § 1.131

We, CAM L. LU, ROBERT B. BENWARE and THAI M. NGUYEN, hereby declare as follows:

1. We are the co-inventors of the invention disclosed and claimed in the subject application Serial No. 10/728,036;

2. We described the invention in the attached paper titled "TRANSITION DELAY FAULTS AND STUCK-AT FAULTS TEST PATTERNS GENERATION FLOW" and in the attached invention disclosure submitted to LSI Logic Corporation for "TRANSITION DELAY FAULT EFFICIENT PATTERN GENERATION FLOW TO ADDRESS HIGH SCAN DATA VOLUME" before the effective date of October 2003 of the publication "High-Frequency, At-Speed Scan Testing" by Lin, et al.;

3. We conceived the invention disclosed in the attached invention disclosure in the United States of America; and

4. We further declare that all statements made herein of our own knowledge are true; and that all statements not based

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on our own knowledge are believed to be true; and further that these statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

_____ /s/_____
DATE SIGNATURE

CAM L. LU

10/19/2005 /s/ RBBenware
DATE SIGNATURE

ROBERT B. BENWARE

_____ /s/_____
DATE SIGNATURE

THAI M. NGUYEN

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on our own knowledge are believed to be true; and further that these statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

10/24/05
DATE

/s/
SIGNATURE

CAM L. LU

DATE

/s/
SIGNATURE

ROBERT B. BENWARE

10/24/05
DATE

/s/
SIGNATURE

THAI M. NGUYEN

LSI LOGIC CONFIDENTIAL

Patent Docket Number - 03-1978 - Transition Delay Fault
Efficient pattern generation flow to address high scan data volume
- Invention Disclosure Acknowledgement - Cam Lu -

Title: Transition Delay Fault Efficient pattern generation flow to address high scan data volume

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Dates

Conception [redacted] Reduction to practice : [redacted]

Disclosure of invention	[redacted]	NDA	Third Party	Mentor Graphic
		NDA	Third Party	VTS

Sale or offer for sale of Invention

Use of Invention [redacted]

Background of Invention

Existing problems: To fit both stuck-at fault (SAF) and transition delay fault (TDF) scan patterns in a semiconductor production test (with fixed amount of scan memory) to achieve highest possible SAF and TDF test coverage.

Existing solutions to these problems: Generate SAF patterns first. Check how much scan memory left. Generate enough TDF pattern to fit into the remaining scan memory.

Disadvantages of existing solutions: Both SAF test coverage could not be maximize in a fixed amount of scan memory.

Description of Invention

Details of Invention: This invention defines how to truncate the generated TDF pattern set such that there is enough scan memory left for the top-off stuck-at pattern set to achieve highest possible coverage. The TDF coverage

[redacted]

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

I/We believe myself (ourselves) to be the first and original inventor(s) of this invention, which was developed during the course of employment. I/We submit this invention disclosure in confidence to attorneys of the LSI Logic IP Law Dept. for the purpose of obtaining a legal opinion and/or advice as to availability of patent, trade secret, and/or copyright protection related to the material contained within.

Inventor(s) [redacted]

Date [redacted]

Witnesses who have read and understood the invention

Witness #1 [redacted]

Date [redacted]

Witness #2 [redacted]

Date [redacted]

LSI LOGIC CONFIDENTIAL

Patent Docket Number - 03-1978 - Transition Delay Fault
Efficient pattern generation flow to address high scan data volume
- Invention Disclosure Acknowledgement - Cam Lu -

will be highest possible provided the selected TDF patterns fit into the scan memory on the selected tester. When TDF patterns are truncated, the corresponding TDF and stuck-at test coverages decrease. Consequently, it will need more top-off stuck-at patterns to achieve highest possible coverage. The truncation algorithm and flow proposed below is based on the assumption that delay defects occur randomly in semiconductor fabrication process. Furthermore The probability of fault A existed in location A is the same as that of fault B existed in location B. The advantages of the the invention always maximizes the test coverage for both TDF and stuck-at tests on the selected tester and the flow can be automated in software.

Features of invention

- Generate Transition delay fault scan patterns first because they can be used for stuck-at fault testing.
- Generate transition delay fault scan patterns based on each clock domain so that they can be tested at the clock domain frequency.
- Truncate generated TDF patterns to minimum to achieve 99.9% defect coverage.
- Only top-off stuck-at fault patterns are needed to achieve highest possible SAF test coverage.

Advantages of invention

- Only patterns that detects 90% of the detected TDF faults are needede to have a 99% defect coverage.
- Always achieve highest possible TDF and SAF test coverages.
- The invented flow was developed based on software automation in mind.
- The processes can distributed and run simultaneously to save pattern generation time.
- No looping is required in the invented flow.

Alternate ways to make or use Invention

The invented flow can be automated in 3rd party ATPG tools.

Other

Prior Art:

[redacted]

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

I/We believe myself (ourselves) to be the first and original inventor(s) of this invention, which was developed during the course of employment. I/We submit this invention disclosure in confidence to attorneys of the LSI Logic IP Law Dept. for the purpose of obtaining a legal opinion and/or advice as to availability of patent, trade secret, and/or copyright protection related to the material contained within.

Inventor(s)

Date

[redacted]

Witnesses who have read and understood the invention

Witness #1

Date

[redacted]

Witness #2

Date

[redacted]

LSI LOGIC CONFIDENTIAL

Patent Docket Number - 03-1978 - Transition Delay Fault Efficient pattern generation flow to address high scan data volume
- Invention Disclosure Acknowledgement - Cam Lu -

Third party issues: Mentor Graphic reviewed the invented flow.
Presented the invented flow as part of a white pattern to VTS (VLSI Test Symposium)

[redacted]

I/We believe myself (ourselves) to be the first and original inventor(s) of this invention, which was developed during the course of employment. I/We submit this invention disclosure in confidence to attorneys of the LSI Logic IP Law Dept. for the purpose of obtaining a legal opinion and/or advice as to availability of patent, trade secret, and/or copyright protection related to the material contained within.

Inventor(s)

Date [redacted]

Witnesses who have read and understood the invention

Witness #1 Date [redacted]

Witness #2 Date [redacted]

Transition Delay Faults

and

Stuck-at Faults

Test Patterns Generation Flow

Cam Lu

Thai Nguyen

Revision 2.0

Proposed TDF and Stuck-at Patterns Generation Flow

1.0 High Scan Test Data Volume Challenge

Scan based TDF and stuck-at testing requires large number (over 30,000 in some designs) of patterns to achieve high test coverage. If TDF testing becomes a LSI production requirement, the challenge is to fit both the TDF and stuck-at patterns into scan memory on production testers. A methodology and a flow need to be defined to address the high pattern count issue.

Mentor had presented the overall performance improvement for Q4 2002 FastScan. For TDF patterns generation, the average run time improvement is 12.1X and the average pattern compression improvement is 2.2X.

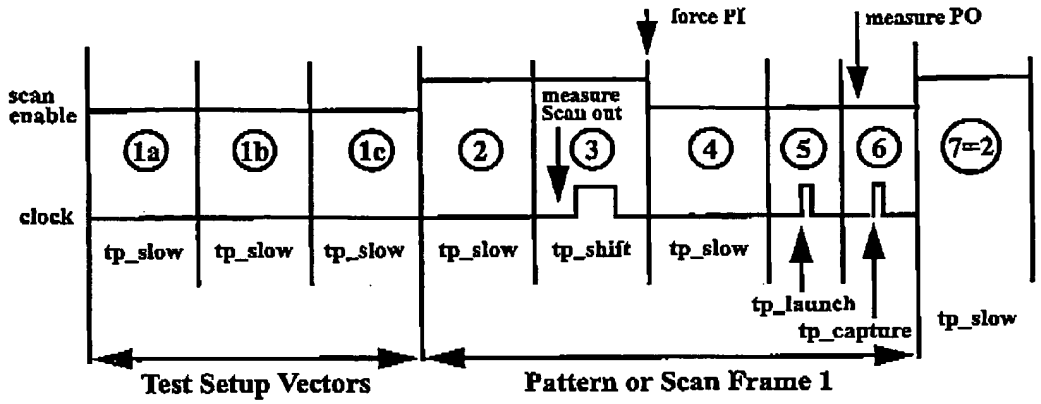
TDF pattern generation time is improved dramatically. For the Pandion design, run time is reduced from 28H:35M to 5H:18M. However, the TDF pattern count is reduced moderately from 28204 to 23857 with about 83.00% test coverage.

2.0 Design Requirements

A TDF testing requirement is to test all clock domains in the design at functional or highest tester speed. DO NOT mux internal clocks of different frequency to the same external clock during scan. Please refer to the "Clock Muxing for Transition Delay Faults Testing" document for more detail information.

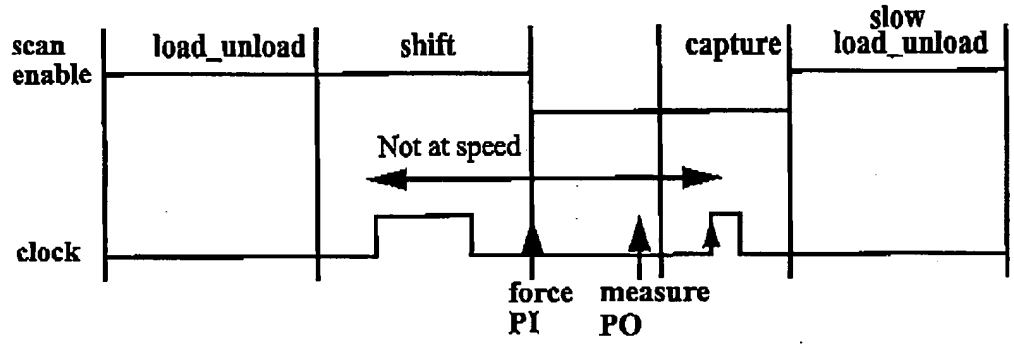
3.0 Stuck-at and TDF Testing Requirements

TDF testing will be required for all future designs. However, the stuck-at fault testing with 99%+ (or highest possible) test coverage requirement remains the highest priority. It means that the final scan pattern set, which contains both TDF patterns and stuck-at patterns, should achieve 99%+ (or highest possible) stuck-at test coverage. TDF test coverage should be as high as possible provided the final pattern set can be fit into the remaining scan memory. All TDF patterns should be generated using the BROADSIDE method as shown below and running at functional or highest tester speed.



4.0 Stuck-at Patterns Detect No Transition Delay Faults

The current stuck-at scan pattern can not be used for TDF testing because the last shift clock and the capture clock are separated by one cycle as shown in the figure below.



5.0 TDF Patterns Detect Stuck-at Faults

TDF patterns, on the other hand, also have stuck-at fault coverage. By definition, to detect a transition delay fault, its corresponding stuck-at fault must be detected. It makes sense to generate TDF patterns first because the same pattern detect both TDF and stuck-at faults. The generated TDF patterns can be fault graded for stuck-at coverage. Then, top-off patterns can be generated to achieve 99%+ (or highest possible) stuck-at coverage.

What happen if the total TDF pattern count exceeds the limit of scan memory allowed by the selected tester?

6.0 Methods to Reduce Scan Test Data Volume

Three (there are more) possible methods to reduced the total scan pattern count were evaluated. Each method is described in detail in the sections followed.

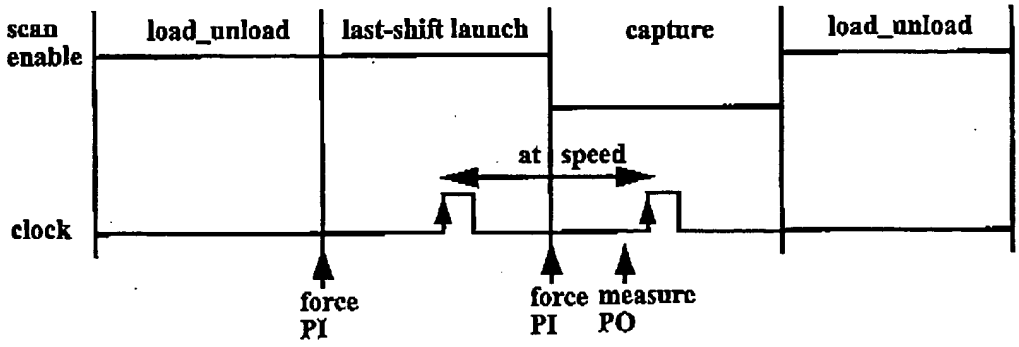
6.1 Use Mentor TestKompress

The Mentor TestKompress tool has capability to reduce scan pattern count up to 10X with test logic inserted into the design to perform the data compaction. Currently there is a lack of resource to qualify and deploy this tool. Also, there is a high cost associate with TestKompress. Due to these reasons, we are not going to see TestKompress in the next 6-9 months at the minimum, unless priorities change.

6.2 Use Launch-off Shift Method to Generate TDF Patterns

The launch-off shift TDF generation method is proven to generate less TDF patterns with higher coverage because transitions are launched during shift. For the Pandion design, only 8234 patterns were generated with 90.09% test coverage compared to 23857 patterns with 83.00% test coverage using the broadside method.

In order to use the launch-off shift method to generate TDF patterns, the global scan enable signal needs to be routed as clock and to have well controlled insertion delay relationship with all other clocks. This method uses the last shift clock as the launch clock as shown in figure below. The global scan enable signal has to be low before the at speed capture clock arrives in the following cycle. Unless the global scan enable signal is laid out with the above requirements, this method can not be used to generate TDF patterns.



6.3 Select Patterns with Maximum Stuck-at and Highest Possible TDF Coverage

This method proposes truncating the generated TDF pattern set such that there is enough scan memory left for the top-off stuck-at pattern set to achieve 99%+ (or highest possible) coverage. The TDF coverage will be highest possible provided the selected TDF patterns fit into the scan memory on the selected tester.

When TDF patterns are truncated, the corresponding TDF and stuck-at test coverages decrease. Consequently, it will need more top-off stuck-at patterns to achieve 99+% (or highest possible) coverage. Keep in mind that stuck-at testing with 99%+ (or highest possible) test coverage requirement remains the highest priority in LSI production test flow.

The truncation algorithm and flow proposed below is based on the assumption that delay defects occur randomly in semiconductor fabrication process. Furthermore The probability of fault A existed in location A is the same as that of fault B existed in location B.

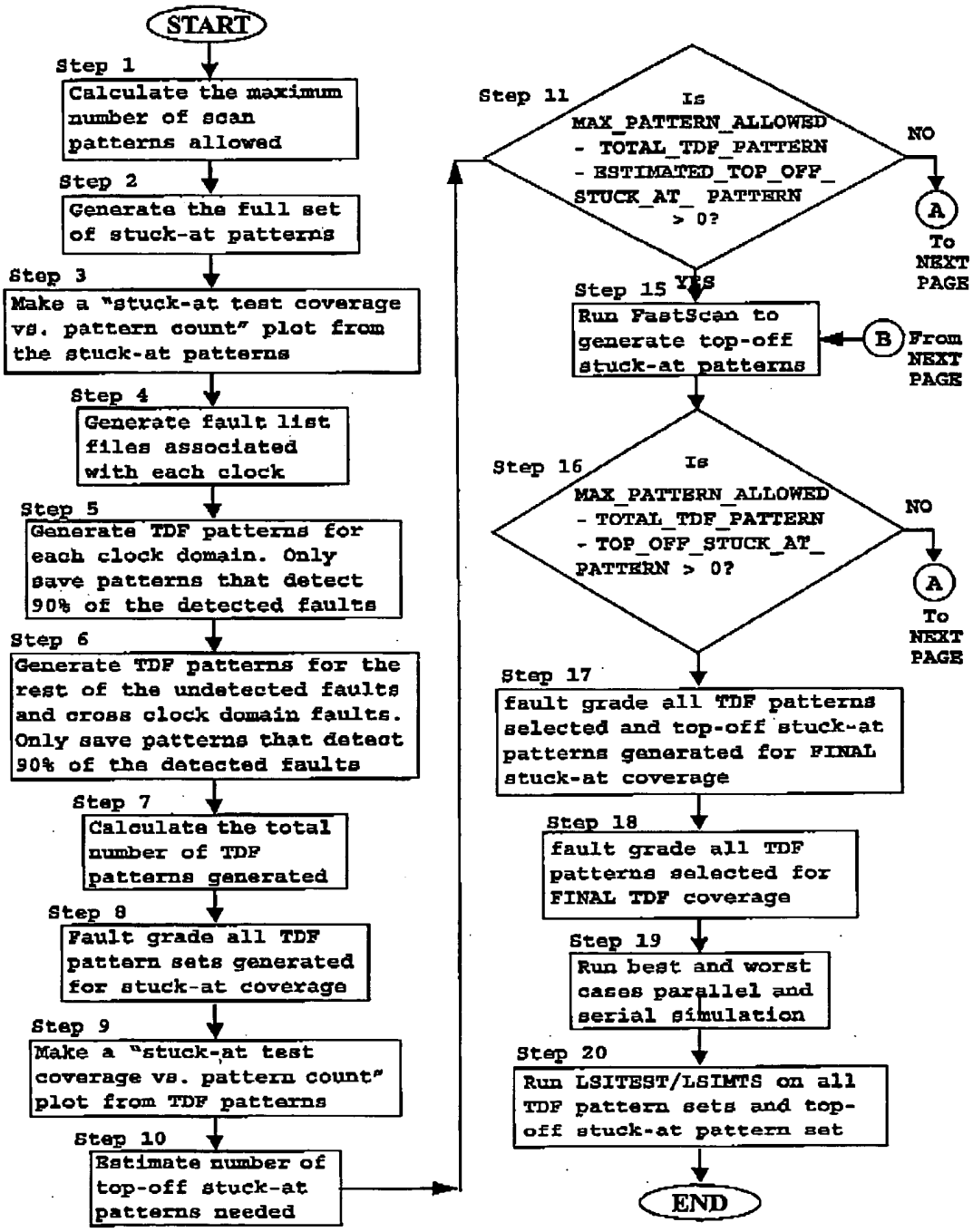
There are both advantage and disadvantage for the proposed algorithm.

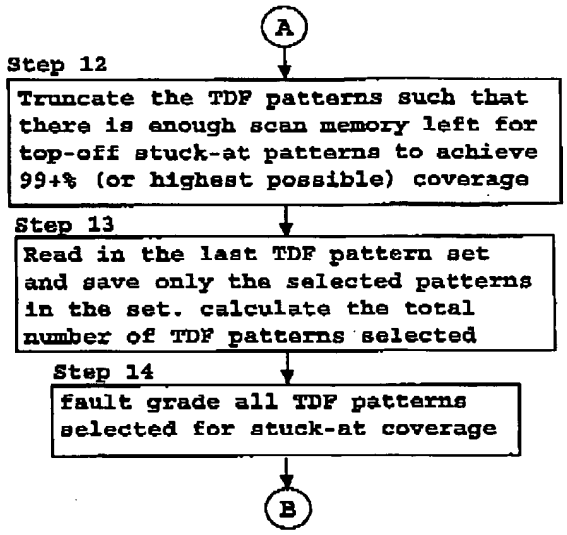
The advantages are it always maximizes the test coverage for both TDF and stuck-at tests on the selected tester and the flow can be automated in FAST. The disadvantages are the test time will be long and it does not take other factors like frequency, voltage, and temperature into account. However, the flow can be fine tuned as we continue to collect and analyze TDF defect data from experiments and production designs.

7.0 Proposed TDF and Stuck-at Pattern Generation Flow

The proposed steps to generate both TDF and stuck-at fault patterns that will fit into the selected tester scan memory are described below.

7.1 TDF and SAF Patterns Generation Flow Chart



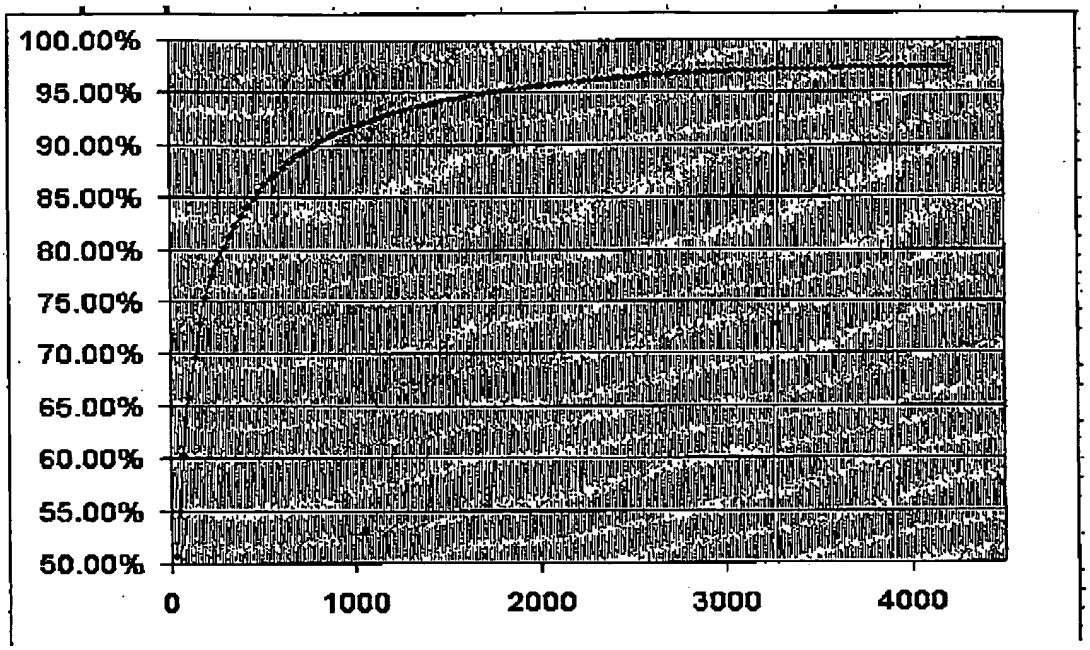


7.2 Step by Step Flow Description

1. **Calculate the maximum number of scan patterns allowed by the selected tester and name it MAX_PATTERN_ALLOWED. Be aware that a portion of the scan memory should be allocated for scan IDDQ and BISR scan tests.**
   - It takes both scan memory and functional (parallel) memory to store one scan pattern. The amount of scan memory needs to store a stuck-at pattern and a TDF pattern is the same. However, it takes one more functional (parallel) memory location to store a TDF pattern compared to stuck-at pattern. Functional (parallel) memory, however, does not appear to be an issue in scan testing.
   - Please refer to the "Memory Calculations for Scan Testing with Hardware Tester" document on ASKK and work with your test engineer to complete this step.
2. **Run FastScan to generate the full set of stuck-at patterns. Make sure all patterns pass best/worst and parall/serial simulations. Find out the pattern count and name it TOTAL_stuck_at_PATTERN.**
   - Always use the "order pattern 3" command to re-order the patterns such that the patterns detected the most faults are placed at the beginning.
   - Run best and worst cases parallel simulation on all stuck-at patterns. Debug if there is mismatch.

- Run best and worst cases serial simulation for 5 stuck-at patterns. Debug if there is mismatch.

3. **Make a "stuck-at test coverage vs. pattern count" plot from result in step 2. A sample plot is shown below.**



- The 1st, 4th, 7th, and 10th data columns shown below are the stuck-at pattern number (From FastScan log file).
- The 2nd, 5th, 8th, and 11th data columns shown below are the stuck-at test coverage (From FastScan log file).
- The 3rd, 6th, 9th, and 12th data columns shown below are the number of patterns needed to get to the highest stuck-at test coverage from the current coverage (calculated).

32	50.71%	4179	1088	92.37%	3123	2144	95.97%	2067	3200	97.14%	1011
64	60.29%	4147	1120	92.55%	3091	2176	96.02%	2035	3232	97.17%	979
96	65.85%	4115	1152	92.77%	3059	2208	96.08%	2003	3264	97.20%	947
128	69.67%	4083	1184	92.93%	3027	2240	96.14%	1971	3296	97.22%	915
160	73.00%	4051	1216	93.12%	2995	2272	96.17%	1939	3328	97.23%	883
192	75.47%	4019	1248	93.27%	2963	2304	96.23%	1907	3360	97.24%	851
224	77.42%	3987	1280	93.43%	2931	2336	96.27%	1875	3392	97.25%	819
256	78.96%	3955	1312	93.57%	2899	2368	96.31%	1843	3424	97.26%	787
288	80.22%	3923	1344	93.73%	2867	2400	96.36%	1811	3456	97.28%	755
320	81.37%	3891	1376	93.86%	2835	2432	96.41%	1779	3488	97.29%	723
352	82.30%	3859	1408	93.97%	2803	2464	96.45%	1747	3520	97.30%	691

384	83.22%	3827	1440	94.09%	2771	2496	96.49%	1715	3552	97.32%	659
416	84.04%	3795	1472	94.21%	2739	2528	96.56%	1683	3584	97.33%	627
448	84.86%	3763	1504	94.31%	2707	2560	96.61%	1651	3616	97.34%	595
480	85.55%	3731	1536	94.41%	2675	2592	96.64%	1619	3648	97.35%	563
512	86.24%	3699	1568	94.52%	2643	2624	96.67%	1587	3680	97.35%	531
544	86.79%	3667	1600	94.61%	2611	2656	96.71%	1555	3712	97.36%	499
576	87.29%	3635	1632	94.72%	2579	2688	96.75%	1523	3744	97.37%	467
608	87.84%	3603	1664	94.82%	2547	2720	96.78%	1491	3776	97.37%	435
640	88.30%	3571	1696	94.90%	2515	2752	96.80%	1459	3808	97.38%	403
672	88.68%	3539	1728	95.00%	2483	2784	96.84%	1427	3840	97.39%	371
704	89.08%	3507	1760	95.09%	2451	2816	96.87%	1395	3872	97.39%	339
736	89.47%	3475	1792	95.18%	2419	2848	96.90%	1363	3904	97.40%	307
768	89.85%	3443	1824	95.27%	2387	2880	96.92%	1331	3936	97.41%	275
800	90.18%	3411	1856	95.34%	2355	2912	96.94%	1299	3968	97.42%	243
832	90.51%	3379	1888	95.43%	2323	2944	96.96%	1267	4000	97.42%	211
864	90.76%	3347	1920	95.51%	2291	2976	97.00%	1235	4032	97.43%	179
896	91.03%	3315	1952	95.58%	2259	3008	97.03%	1203	4064	97.43%	147
928	**91.30%**	**3283**	1984	95.66%	2227	3040	97.05%	1171	4096	97.44%	115
960	91.51%	3251	2016	95.73%	2195	3072	97.06%	1139	4128	97.44%	83
992	91.76%	3219	2048	95.79%	2163	3104	97.08%	1107	4160	97.45%	51
1024	91.95%	3187	2080	95.86%	2131	3136	97.10%	1075	4192	97.45%	19
1056	92.16%	3155	2112	95.91%	2099	3168	97.12%	1043	4211	97.45%	0

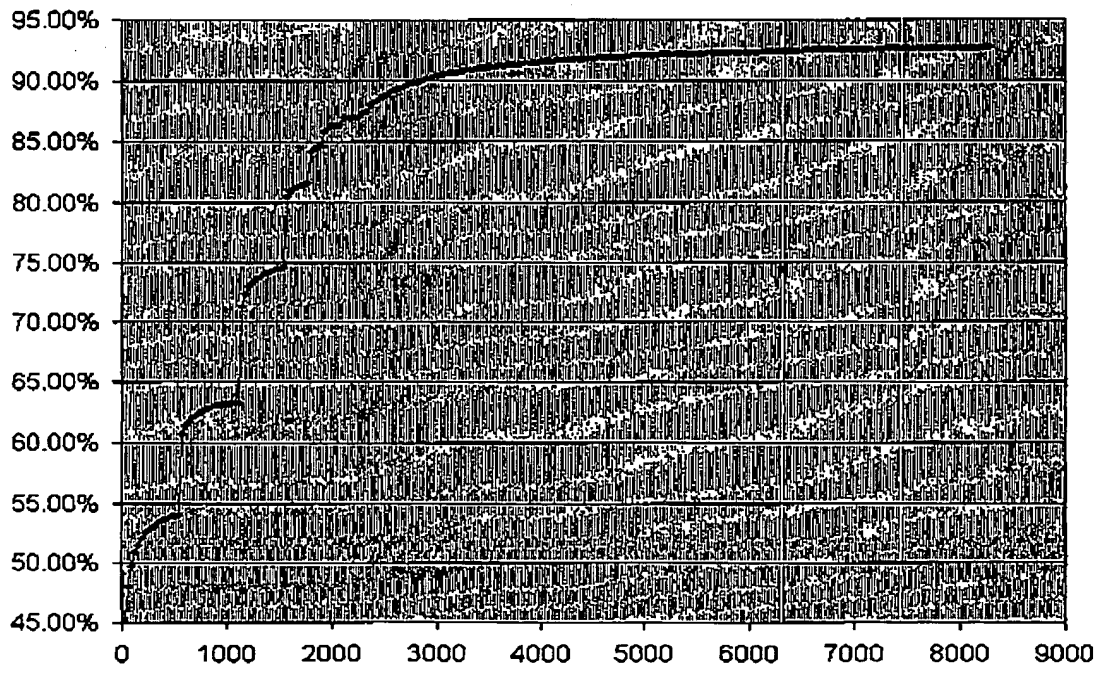
4. **Run FastScan to generate fault list files associated with every scan clock using the "write classified faults" command.**
   - For scan sets and scan resets declared as scan clocks, constrain them to their inactive values because they do not capture transition faults into scan cells.
   - When this command is used, FastScan lists all faults that can be captured by each clock in a file. For a design with N scan clocks, N+1 fault list files will be generated. The last file contains faults that can not be captured by any scan clock.
5. **Run FastScan to generate TDF patterns for each scan clock. If there are 200 or less patterns generated for a clock domain, do not bother to truncate them. If there are more than 200 patterns generated, calculate the total number of faults detected and save only the patterns that detect 90% of the detected faults in the run.**
   - For scan sets and scan resets declared as scan clocks, constrain them to their inactive values because they do not capture transition faults into scan cells.
   - Enable all scan clocks during shifting, but only the targeted scan clock during launching and capturing.

- Load only the faults associated with the targeted scan clock.
- Each run detects transition delay faults within the targeted clock domain. For example, a fault that is launched by scan clock A and capture by scan clock A.
- Run time should be very fast for small clock domain.
- Run time should be reasonable for any large clock domains because only faults associated with the targeted clock domain are submitted in the run.
- All runs in this step can be started simultaneously if licenses are available.
- The generated TDF patterns should be able to run at functional speed for the launch and capture cycles.
- Always use the "order pattern 3" command to re-order the patterns such that the patterns that detected the most faults are at the beginning.
- Based on TDF data collected and analyzed by the Advanced Defects Screening group, with TDF patterns that detect 90% of the faults in each clock, 99.9% of TDF defect parts are screened out. However, the total TDF patterns are reduced by about 75%. Note that in almost every case, TDF patterns need to be truncated to fit into the scan memory. There will always be test escaped parts, but the goal is to keep the test escaped parts to minimum with affordable test cost.
- Save all ASCII, VERILOG test bench and WGL files. There is no need to generate any serial VERILOG test bench and serial WGL files.
- Save all detected and undetected faults for each run.

6. **Run FastScan to generate TDF patterns for the rest of the undetected faults and cross clock domain faults. If there are 200 or less patterns generated for a clock domain, do not bother to truncate them. If there are more than 200 patterns generated, calculate the total number of faults detected and save only the patterns that detect 90% of the detected faults in the run.**
   - Enable all scan clocks for shifting, launching, and capturing.
   - Load the n+1 fault list generated in step 4.
   - Load all the undetected faults reported from runs in step 5.
   - This run detects transition delay faults across clock domain. For example, a fault that is launched by scan clock A and capture by scan clock B.
   - Run time will be longer than any run in step 5.

- The generated TDF patterns can only be run at the slowest scan clock speed for the launch and capture cycles.
- Always use the "order pattern 3" command to re-order the patterns such that the patterns that detected the most faults are at the beginning.
- Save all ASCII, VERILOG test bench and WGL files. There is no need to generate any serial VERILOG test bench and serial WGL files.
- Very likely, this pattern set needs to be truncated to fit into the scan memory.

7. **Calculate the total number of TDF patterns generated in steps 5 and 6 and name it TOTAL_TDF_PATTERN.**
8. **Run FastScan to fault grade all TDF pattern sets generated in steps 5 and 6 for stuck-at coverage.**
   - It is very important to order the TDF pattern sets from the largest to the smallest in this step because highest stuck-at coverage can be achieved in this arrangement. Patterns in the smaller patterns are more likely to be truncated based on the proposed algorithm.
   - Save all detected and undetected faults.
9. **Make a "stuck-at test coverage vs.pattern count" plot from result in step 8. A sample plot is shown below.**



- The 1st, 4th, 7th, and 10th data columns shown below are the stuck-at pattern number (From FastScan log file).
- The 2nd, 5th, 8th, and 11th data columns shown below are the stuck-at test coverage (From FastScan log file).
- The 3rd, 6th, 9th, and 12th data columns shown below are the number of patterns can be added before hitting the maximum number patterns allowed by the selected tester (Calculated based on the assumption that 7K is the maximum scan patterns allowed in this example).

32	45.22%	6968	2123	86.98%	4877	4194	91.70%	2806	6306	92.46%	694
64	48.01%	6936	2155	86.99%	4845	4226	91.71%	2774	6338	92.46%	662
96	49.80%	6904	2187	87.00%	4813	4258	91.76%	2742	6370	92.47%	630
128	50.92%	6872	2219	87.00%	4781	4290	91.78%	2710	6402	92.48%	598
160	51.48%	6840	2251	87.00%	4749	4322	91.80%	2678	6434	92.48%	566
192	52.09%	6808	2283	87.36%	4717	4354	91.82%	2646	6466	92.49%	534
224	52.54%	6776	2315	87.38%	4685	4386	91.84%	2614	6498	92.49%	502
256	52.79%	6744	2334	87.38%	4666	4418	91.85%	2582	6530	92.50%	470
288	53.02%	6712	2362	87.90%	4638	4450	91.87%	2550	6562	92.50%	438
320	53.18%	6680	2370	88.02%	4630	4482	91.88%	2518	6594	92.51%	406
352	53.47%	6648	2402	88.20%	4598	4514	91.91%	2486	6626	92.51%	374
384	53.61%	6616	2434	88.36%	4566	4546	91.92%	2454	6658	92.52%	342
416	53.71%	6584	2466	88.54%	4534	4578	91.93%	2422	6690	92.52%	310
448	53.84%	6552	2498	88.73%	4502	4610	91.94%	2390	6722	92.52%	278
480	53.95%	6520	2530	88.87%	4470	4642	91.96%	2358	6754	92.52%	246
512	54.02%	6488	2562	89.01%	4438	4674	91.97%	2326	6786	92.53%	214
544	54.09%	6456	2594	89.16%	4406	4706	91.98%	2294	6818	92.53%	182
576	60.68%	6424	2626	89.31%	4374	4738	92.00%	2262	6850	92.54%	150
608	61.41%	6392	2658	89.41%	4342	4770	92.01%	2230	6882	92.54%	118
640	61.82%	6360	2690	89.55%	4310	4802	92.02%	2198	6914	92.55%	86
672	62.11%	6328	2722	89.66%	4278	4834	92.03%	2166	6946	92.55%	54
704	62.30%	6296	2754	89.76%	4246	4866	92.04%	2134	6978	92.56%	22
736	62.50%	6264	2786	89.85%	4214	4898	92.04%	2102	7010	92.56%	-10
768	62.65%	6232	2818	89.92%	4182	4930	92.05%	2070	7042	92.57%	-42
800	62.78%	6200	2850	90.01%	4150	4962	92.06%	2038	7074	92.58%	-74
832	62.85%	6168	2882	90.10%	4118	4994	92.08%	2006	7106	92.59%	-106
864	62.93%	6136	2914	90.18%	4086	5026	92.09%	1974	7138	92.60%	-138
896	63.01%	6104	2946	90.25%	4054	5058	92.10%	1942	7170	92.60%	-170
928	63.09%	6072	2978	90.33%	4022	5090	92.11%	1910	7202	92.61%	-202
960	63.14%	6040	3010	90.39%	3990	5122	92.13%	1878	7234	92.61%	-234
992	63.18%	6008	3042	90.47%	3958	5154	92.15%	1846	7266	92.61%	-266
1024	63.23%	5976	3074	90.52%	3926	5186	92.15%	1814	7298	92.62%	-298
1056	63.25%	5944	3106	90.59%	3894	5218	92.16%	1782	7330	92.62%	-330
1088	63.28%	5912	3138	90.64%	3862	5250	92.17%	1750	7362	92.62%	-362
1120	63.31%	5880	3170	90.70%	3830	5282	92.18%	1718	7394	92.62%	-394
1152	71.29%	5848	3202	90.74%	3798	5314	92.18%	1686	7426	92.63%	-426

1184	72.36%	5816	3234	90.78%	3766	5346	92.19%	1654	7458	92.63%	-458
1216	72.93%	5784	3266	90.83%	3734	5378	92.20%	1622	7490	92.63%	-490
1248	73.31%	5752	3298	90.89%	3702	5410	92.21%	1590	7522	92.64%	-522
1280	73.59%	5720	3330	90.93%	3670	5442	92.22%	1558	7554	92.65%	-554
1312	73.81%	5688	3362	90.97%	3638	5474	92.23%	1526	7586	92.65%	-586
1344	74.01%	5656	3394	91.02%	3606	5506	92.24%	1494	7618	92.65%	-618
1376	74.14%	5624	3426	91.05%	3574	5538	92.25%	1462	7650	92.66%	-650
1408	74.26%	5592	3458	91.08%	3542	5570	92.26%	1430	7682	92.66%	-682
1440	74.35%	5560	3490	91.13%	3510	5602	92.27%	1398	7714	92.66%	-714
1472	74.45%	5528	3522	91.17%	3478	5634	92.28%	1366	7746	92.67%	-746
1504	74.53%	5496	3554	91.20%	3446	5666	92.29%	1334	7778	92.67%	-778
1536	74.60%	5464	3586	91.23%	3414	5698	92.29%	1302	7810	92.67%	-810
1568	80.41%	5432	3618	91.26%	3382	5730	92.30%	1270	7842	92.68%	-842
1600	80.89%	5400	3650	91.29%	3350	5762	92.31%	1238	7874	92.68%	-874
1632	81.13%	5368	3682	91.33%	3318	5794	92.31%	1206	7906	92.68%	-906
1664	81.28%	5336	3714	91.35%	3286	5826	92.32%	1174	7938	92.69%	-938
1696	81.39%	5304	3746	91.38%	3254	5858	92.32%	1142	7970	92.69%	-970
1728	81.48%	5272	3778	91.42%	3222	5890	92.33%	1110	8002	92.69%	-1002
1760	81.55%	5240	3810	91.44%	3190	5922	92.34%	1078	8034	92.70%	-1034
1792	84.11%	5208	3842	91.46%	3158	5954	92.34%	1046	8066	92.70%	-1066
1824	84.37%	5176	3874	91.49%	3126	5986	92.34%	1014	8098	92.70%	-1098
1856	84.51%	5144	3906	91.51%	3094	6018	92.35%	982	8130	92.71%	-1130
1888	84.59%	5112	3938	91.54%	3062	6050	92.35%	950	8162	92.71%	-1162
1920	85.79%	5080	3970	91.56%	3030	6082	92.36%	918	8194	92.72%	-1194
1952	86.07%	5048	4002	91.58%	2998	6114	92.41%	886	8226	92.72%	-1226
1984	86.22%	5016	4034	91.61%	2966	6146	92.42%	854	8258	92.73%	-1258
2016	86.31%	4984	4066	91.62%	2934	6178	92.43%	822	8290	92.73%	-1290
2048	86.38%	4952	4098	91.64%	2902	6210	92.44%	790			
2080	86.43%	4920	4130	91.66%	2870	6242	92.44%	758			
2112	86.93%	4888	4162	91.68%	2838	6274	92.45%	726			

10. **Estimate the number of top-off stuck-at patterns needed, ESTIMATED_TOP_OFF_STUCK_AT_PATTERN, based on the analysis from step 9 and step 3.**

11. **If MAX_PATTERN_ALLOWED - TOTAL_TDF_PATTERN - ESTIMATED_TOP_OFF _STUCK_AT_PATTERN > 0. All TDF patterns and top-off stuck-at patterns should fit into the selected tester scan memory. Go to step 15. Otherwise, it is necessary to truncate the TDF patterns by following the next step.**

12. **Truncate the TDF patterns such that is enough memory left to generate top-off stuck-at pattern to achieve 99+% (or highest possible) coverage. Please refer to the plots and data in step 3 and step 9 for the analysis below. Examples are show below.**

    - Data point 1: Based on the plot in step 9, if truncating the TDF pattern set at 3650, the corresponding stuck-at coverage is 91.29%. There is space for 3350 top-off patterns. Based

on the plot in step 3, from 91.03%, 3315 patterns are needed to achieve 97.45% test coverage. However, there is still space for 35 patterns before hitting the maximum 7K limit.

- Data point 2: Based on the plot in step 9, if truncating the TDF pattern set at 3682, the corresponding stuck-at coverage is 91.33%. There is space for 3318 top-off patterns. Based on the plot in step 3, from 91.30%, 3283 patterns are needed to achieve 97.45% test coverage. However, there is still space for 35 patterns before hitting the maximum 7K limit.
- Data point 3: Based on the plot in step 9, if truncating the TDF pattern set at 3714, the corresponding stuck-at coverage is 91.35%. There is space for 3286 top-off patterns. Based on the plot in step 3, from 91.30%, 3283 patterns are needed to achieve 97.45% test coverage. However, there is still space for 3 patterns before hitting the maximum 7K limit. **(RECOMMENDED)**
- Data point 4: Based on the plot in step 9, if truncating the TDF pattern set at 3746, the corresponding stuck-at coverage is 91.38%. There is space for 3254 top-off patterns. Based on the plot in step 3, from 91.30%, 3283 patterns are needed to achieve 97.45% test coverage. There is not enough space (29 patterns space short) for the top-off stuck-at patterns.
- Data point 5: Based on the plot in step 9, if truncating the TDF pattern set at 3778, the corresponding stuck-at coverage is 91.42%. There is space for 3222 top-off patterns. Based on the plot in step 3, from 91.30%, 3283 patterns are needed to achieve 97.45% test coverage. There is not enough space (61 patterns space short) for the top-off stuck-at patterns.

13. Run FastScan to truncate the last TDF pattern set by saving only the selected patterns in the set. Calculate the total number of TDF patterns selected and name it TDF_PATTERN_SELECTED.

- For example, if there are 11 TDF pattern sets and only 1344 out of 5920 patterns in the last pattern set are selected. Run FastScan to read in the ASCII file of the last pattern set and save only the first 1344 patterns.
- There also can be cases that a few small TDF pattern sets needed to be removed due to scan memory limit.

14. Run FastScan to fault grade all TDF patterns selected for stuck-at coverage.

- Save all detected and undetected faults.

15. Run FastScan to generate top-off stuck-at patterns to achieve 99+% (or highest possible) coverage. Find out the pattern count and name it TOP_OFF_STUCK_AT_PATTERN.
    - Load only the undetected faults
    - Save the ASCII, all patterns parallel VERILOG test bench, five patterns serial VERILOG test bench, and WGL files.
16. If MAX_PATTERN_ALLOWED - TDF_PATTERN_SELECTED - TOP_OFF_STUCK_AT_PATTERN > 0, both the TDF patterns and the top-off stuck-at patterns indeed fit into the selected tester scan memory. Otherwise, it is necessary to truncate TDF patterns by looping back to step 12.
17. Run FastScan to fault grade all TDF patterns selected and top-off stuck-at patterns generated for stuck-at coverage. The result is the final stuck-at coverage for the design.
18. Run FastScan to fault grade all TDF patterns selected for TDF coverage. The result is the final TDF coverage for the design.
19. Run best and worst cases parallel simulation on all TDF patterns and the top-off stuck-at patterns. Debug if there is mismatch. Run best and worst cases serial simulation for 5 stuck-at patterns. Debug if there is mismatch.
20. Run LSITEST and LSIMTS on all TDF pattern sets and top-off stuck-at pattern set to perform tester rules, bidirectional conflicts checking, and generate test program. Debug if there is violation.

8.0 Stuck-at Test Coverage Varies In Different ATPG Setup

There are many ways to setup an ATPG run. Depending on commands used and the pattern generation flow, the result may varies. Some FastScan commands and pattern generation flows known to have affect in test coverage and pattern count are shown below.

- set abort limit N
- set split capture_cycle on/off
- set simulation mode combination -depth N
- set atpg limit -pattern_count N -test_coverage M
- restore_bidi and clock procedure vs. capture procedure
- faults submitted to ATPG tool in different order
- fault simulating TDF and top-off patterns for stuck-at coverage

In many cases, the final stuck-at test coverage obtained from the proposed TDF flow may be different (lower) compared to the traditional stuck-at flow. An example is shown below.

Tradition stuck-at test coverage:

testable faults = 944118 - 24842 - 1588 - 418 - 3142 = 914128
(total) (UU) (TI) (BL) (RE)
tested faults = 763705 + 126996 + (1468*0.5) = 891435
(DS) (DI) (PU*credit)
test coverage = 891435 / 914128 = 97.52%

Fault simulating TDF patterns and top-off stuck-at patterns for stuck-at coverage:

testable faults = 944118 - 24842 - 1588 - 418 = 917270
(total) (UU) (TI) (BL)
tested faults = 763855 + 126904 + (1140*0.5) = 891329
(DS) (DI) (PU*credit)
test coverage = 891329 / 917270 = 97.17%

The testable faults in the TDF flow includes the 3142 redundant faults reported in the traditional stuck-at flow because fault simulation was used to calculate the final fault coverage and fault simulation does not identify redundant faults like the ATPG process. If the 3142 redundant faults were removed from the calculation, the test coverage would be 97.50%.

9.0 Study Case 1 – The Pandion Design

Pandion is a 430K-gate, lcbg12p Seagate design. The selected production tester is Credence's DUO(QUARTET).

The design has 10 scan clocks with frequencies as shown below.

Scan Clock Names	Functional Domains	Frequencies
c_gpio[0]	H-Clk	40Mhz/80Mhz
c_gpio[1]	Ref_Clk	40Mhz/60Mhz
c_gpio[2]	UART Clock	48MHz
c_gpio[3]	Osprey C-Clock	48MHz
c_gpio[4]	Osprey S-Clock	40MHz

Scan Clock Names	Functional Domains	Frequencies
c_gpio[5]	ARM Clock	160Mhz
c_gpio[6]	ARM Clock	160Mhz
srv_clk_a_N/P	Servo Clock	100Mhz
askreq	askreq/ETM Clock/H-Clk	40Mhz/160Mhz/80MHz
xtal_in	xtal_in/ARM Clock	160Mhz

The design has 20 scan chains as shown below.

Chain Name	Scan in Name	Scan Out Name	Cell Number
Chain 1	c_gpio[10]	ea[1]	1139
Chain 2	c_gpio[11]	ea[2]	1139
Chain 3	c_gpio[12]	ea[3]	1140
Chain 4	c_gpio[13]	ea[4]	1140
Chain 5	c_gpio[14]	ea[5]	1139
Chain 6	c_gpio[15]	ea[6]	1139
Chain 7	c_gpio[16]	ea[7]	1140
Chain 8	c_gpio[17]	ea[8]	1140
Chain 9	c_gpio[18]	ea[9]	916
Chain 10	c_gpio[19]	ea[10]	879
Chain 11	c_gpio[20]	ea[11]	915
Chain 12	c_gpio[21]	ea[12]	879
Chain 13	c_gpio[22]	ea[13]	1114
Chain 14	c_gpio[23]	ea[14]	1093
Chain 15	c_gpio[24]	ea[15]	1093
Chain 16	c_gpio[25]	ea[16]	816
Chain 17	c_gpio[0]	ea[17]	816
Chain 18	c_gpio[1]	ea[18]	1207
Chain 19	c_gpio[2]	ea[19]	733
Chain 20	c_gpio[3]	ea[20]	611

FastScan version v8_2002_4.10 was used to generate TDF and stuck-at scan patterns.

1. The maximum number of scan patterns allowed by the selected tester, DUO(QUARTET), MAX_PATTERN_ALLOWED = 7K. Scan memory was also reserved for IDDQ patterns.
2. Run FastScan to generate the full set of stuck-at pattern. TOTAL_stuck_at_PATTERN = 4211.
3. Make a "stuck-at test coverage vs. pattern count" plot from result in step 2. The plot and data were shown in step 3 in the "Step by Step Flow Description" section.
4. Run FastScan to generate fault list files associated with every scan clock using the "write classified faults" command.
5. Run FastScan to generate TDF patterns for each scan clock. If there are 200 or less patterns generated for a clock domain, do not bother to truncate them. If there are more than 200 patterns generated, calculate the total number of faults detected and save only the patterns that detect 90% of the detected faults in the run. The scan sets and resets were constrained to their inactive values. 400 MHZ SUN UltraSPARC workstations were used to generate TDF patterns and the results are shown below.

	Scan Clock Names	Original Pattern Number	Truncated Pattern Number	Run Time
1	c_gpio[0]	1231	576	35M
2	c_gpio[1]	498	128	19M
3	c_gpio[2]	83	83	04M
4	c_gpio[3]	8	8	03M
5	c_gpio[4]	28	28	03M
6	c_gpio[5]	298	192	13M
7	c_gpio[6]	1207	416	49M
8	xtal_in	2852	544	03H:23M
9	askrcq	739	224	22M
10	srv_clk_a_N/P	171	171	07M
11	All clocks enabled	16325	5920	06H:39M

	Scan Clock Names	Original Pattern Number	Truncated Pattern Number	Run Time
Total		23440	8290	12H:37M

6. Run FastScan to generate TDF patterns for the rest of the undetected faults and cross clock domain faults. The result is also shown in table above.
7. Calculate the total number of TDF patterns generated in steps 5 and 6 and name it TOTAL_TDF_PATTERN. TOTAL_TDF_PATTERN = 8290.
8. Run FastScan to fault grade all TDF pattern sets generated in steps 5 and 6 for stuck-at test coverage. The test coverage is 92.73%.
9. Make a "stuck-at test coverage vs.pattern count" plot from result in step 6. The plot and data were shown in step 9 in the "Step by Step Flow Description" section.
10. Estimate the number of top-off stuck-at patterns needed. Set ESTIMATED_TOP_OFF_STUCK_AT_PATTERN = 3091 based on the analysis from step 9 and step 3.
    - From step 9, with 8290 TDF patterns, 92.73% stuck-at test coverage is achieved.
    - From step 3, the data shows that it needs at least 3091 patterns (but can be less) to go from 92.73% to the highest stuck-at test coverage of 97.45%.
11. The total number of TDF patterns alone, 8290, exceeds the maximum number of scan patterns allowed (7K). Pattern truncation is needed.
12. Truncate the TDF patterns such that is enough memory left to generate top-off stuck-at pattern to achieve 99+% (or highest possible) coverage. The analysis was shown in step 12 in the "Step by Step Flow Description" section.
13. Run FastScan to truncate the last TDF pattern set by saving only the selected patterns in the set. Calculate the total number of TDF patterns selected. TDF_PATTERN_SELECTED = 3714.
14. Run FastScan to fault grade all TDF patterns selected for stuck-at coverage and save all detected and undetected faults. The test coverage is 91.35%.
15. Run FastScan to generate top-off stuck-at patterns to achieve 99+% (or highest possible) coverage. Find out the pattern count and name it TOP_OFF_STUCK_AT_PATTERN = 2313.

16. Both the TDF patterns and the top-off stuck-at patterns indeed fit into the selected tester scan memory. The total TDF and stuck-at pattern count is 6027 which is 973 less than the maximum 7K allowed by the selected tester.
17. Run FastScan to fault grade all TDF patterns selected for TDF coverage. 74.94% is the final TDF coverage for the design.
18. Run FastScan to fault grade all TDF patterns selected and top-off stuck-at patterns generated for stuck-at coverage. 97.52% is the final stuck-at coverage for the design.
19. All best and worst cases parallel and serial simulations for TDF patterns and the top-off stuck-at patterns passed.
20. Run LSITEST and LSIMTS successfully on all TDF pattern sets and the top-off stuck-at pattern set.

LSI Logic Intellectual Property Law Department Memo
Date: Thursday, October 02, 2003
LSI Docket Number: 03-1978

Title : Transition Delay Fault Efficient pattern generation flow to address high scan data volume

Subject: Patent - 03-1978 - - - PLEASE ARRANGE FOR A CONFERENCE WITH THE INVENTOR(S) AND WATCH OUT FOR BAR DATES! - Transition Delay Fault Efficient pattern
generation flow to address high scan da

An invention disclosure has been sent to you for drafting patent application.

Please arrange for a conference with the inventor(s) to ensure that you have a complete understanding of the details of the invention as contained in the invention disclosure sent to you.

Additionally, please ensure that we are within all bar dates (if any). If the disclosure does not provide for any information on bar dates, please confirm the same with the
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Technology Classification : Test (Chip)

1. EJTAG
1. JTAG
1. Scan testing (general)
1. Test (software)
1. Test mux

2003/09/12 - Award - Disclosure
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inventor(s). **2003/09/12 - Disclosure - Received from Inventor(s)**
2003/09/24 - Commn. from Inventor - Received - Connie,
2003/09/24 - Disclosure - Received signed and witnessed form
2003/09/25 - Disclosure - Received from Attorney with 1st review
2003/09/25 - Disclosure - Sent to Reviewer
2003/09/25 - Commn. from Inventor - Received - Connie,
2003/09/25 - Log - Emailed quicknote - TO : - Paralegal - connie@lsil.com - First
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2003/10/01 - Disclosure - Received from Reviewer - Approved
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2003/11/06 - Due Date - to receive first draft

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File

October 20, 2003

VIA FEDERAL EXPRESS

Mr. Cam L. Lu
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1501 McCarthy Blvd., MS E194
Milpitas, CA 95035

RE: Proposed U.S. Patent Application
Cam et al.; METHOD OF GENERATING A TRUNCATED SCAN TEST PATTERN FOR AN INTEGRATED CIRCUIT DESIGN
LSI Ref. No. 03-1978; Our Ref. No. 81641 (6653)

Dear Cam:

Enclosed herewith for inventor review and comment is a first draft patent application directed to the above-identified subject matter. This application was prepared based upon the information contained in the invention disclosure and from communication with the inventor. Please pay particular attention to the bolded, highlighted areas in the application where further information is needed. Please ensure that all inventors have carefully reviewed and provided comments to the application, red-lining it as necessary to ensure that it accurately and completely describes the invention.

Upon completion of review by all inventors, please return a single red-line copy of the application to us by November 3, 2003 to allow time to make any necessary revisions and order formal drawings in preparation for filing the application with the U.S. Patent & Trademark Office.

The presently identified inventors are listed on the cover sheet of the application. Please confirm whether this is a complete listing of the inventors. All of the inventors must be identified, and each inventor must review the application. In general, for a person to be named as an inventor that person must have contributed to the "conception" of at least one claim in the application. Thus, the claims must be reviewed to determine inventorship. Please give me a call if you would like to discuss inventorship and "conception".

It is important that we provide a complete and accurate description of the invention in the application at the time of filing, as adding new material necessary to understand or practice the invention after filing may jeopardize our ability to rely on the original filing date.

As you review the application, please keep in mind that it must be of sufficient detail to enable a person skilled in the art to make and use the invention. Furthermore, the application must set forth the "best mode" contemplated by the inventors of carrying out their invention. In general, the "best mode" of the invention is the best way known to the inventors of practicing or using the invention.

As you may be aware, each individual associated with the filing or prosecution of a patent application has a duty of candor and good faith to disclose to the U.S. Patent and Trademark Office all information known to that individual to be "material" to the patentability of the invention. This duty continues throughout the prosecution of the application until the application is either abandoned or issued as a patent. Because it is difficult to define whether an item of information is "material", we should err on the side of including in the of which we are aware that appears relevant to the application, including any relevant patents, publications, or acts such as any public use of the invention or sales or offers to sell the invention. Please provide copies of any such information to us. If you are uncertain whether a piece of information is material, please provide us with a copy.

Also please provide copies of any related patent applications, including application serial numbers and filing dates.

I look forward to receiving your comments and revisions. In the meantime, should you have any questions, comments or concerns, please contact me at your earliest convenience.

Sincerely,

FITCH, EVEN, TABIN & FLANNERY

Eric J. Whitesell

EJW/rlm
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cc: R. Wawrzyniak, Esq. (w/ encl.)

JAB164\xcL001

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November 24, 2003

VIA FEDERAL EXPRESS

Ms. Connie del Castillo
LSI Logic Corporation
1551 McCarthy Blvd. MS D-106
Milpitas, CA 95035

RE: Proposed U.S. Patent Application
Cam et al.; METHOD OF GENERATING AN EFFICIENT STUCK-AT FAULT AND TRANSITION DELAY FAULT TRUNCATED SCAN TEST PATTERN FOR AN INTEGRATED CIRCUIT DESIGN
LSI Ref. No. 03-1978; Our Ref. No. 81641 (6653)

Dear Connie:

Enclosed herewith for review and execution by the inventors is a final draft patent application directed to the above-identified invention. This application incorporates comments received from the inventors. Also enclosed in duplicate, per LSI's request, are an Assignment and Declaration/Power of Attorney.

As mentioned previously, each individual associated with the filing or prosecution of a patent application has a duty of candor and good faith to disclose to the U.S. Patent and Trademark Office all information known to that individual to be "material" to the patentability of the invention. This duty continues throughout the prosecution of the application until the application is either abandoned or issued as a patent. Because it is difficult to define whether an item of information is "material", we should err on the side of including any information of which we are aware that appears relevant to the application, including any relevant patents, publications, or acts such as any public use of the invention or sales or offers to sell the invention. Please provide copies of any such information to us. If you are uncertain whether a piece of information is material, please provide us with a copy. Please have each inventor review and initial the paragraph provided on the cover sheet of the enclosed final draft application.

Upon the inventors' review of the final draft patent application, please have the inventors execute both copies of the formal documents, have both copies of the Assignment witnessed, and return them (including the patent application, with initialed cover sheet) to our office by December 10, 2003, at which time we will proceed to file the application and formal documents with the U.S. Patent & Trademark Office.

As always, please do not hesitate to contact us should you have any questions and/or comments relative to the above.

Sincerely,

Eric J. Whitesell

EJW/rlm
Enclosures
cc: R. Wawrzyniak (w/o encls.)

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